CLAIMS:

1. A semiconductor memory device comprising:

a semiconductor die encapsulated in a package, the package having an encapsulating body and electrically conductive interconnect pins extending outwardly from the body;

a total of no more than 68,000,000 functional and operably addressable memory cells arranged in multiple memory arrays formed on the die, the individual functional and operably addressable memory cells occupying area on the die within the memory arrays, the occupied area of all functional and addressable memory cells on the die having a total combined area which is no greater than 53 mm^2; and

peripheral circuitry and pitch circuitry formed on the die relative to the memory arrays; the peripheral circuitry electrically interconnecting with the pins and including operably interconnected control and timing circuitry, address and redundancy circuitry, data and test path circuitry, and voltage supply circuitry which collectively enable full access to all addressable memory cells of the memory arrays.

2. The semiconductor memory device of claim 1 wherein the die is fabricated to include a total of four or less composite conductive line layers.

3. The semiconductor memory device of claim 1 wherein the peripheral circuitry, the pitch circuitry and the memory arrays have a total combined continuous surface area on the die which is less than or equal to 106 mm^2.

4. The semiconductor memory device of claim 1 wherein the peripheral circuitry, the pitch circuitry, and the memory arrays are fabricated to include at least five composite conductive line layers, the occupied area of all functional and operable memory cells on the die having a total combined area on the die which is no greater than 40 mm^2.

5. The semiconductor memory device of claim 1 wherein the peripheral circuitry, the pitch circuitry, and the memory arrays are fabricated to include at least five composite conductive line layers; the peripheral circuitry, the pitch circuitry and the memory arrays having a total combined continuous surface area on the die which is less than or equal to 93 mm^2.

6. A semiconductor memory device comprising:

a semiconductor die encapsulated in a package, the package having an encapsulating body and electrically conductive interconnect pins extending outwardly from the body;

a total of no more than 17,000,000 functional and operably addressable memory cells arranged in multiple memory arrays formed on the die, the individual functional and operably addressable memory cells occupying area on the die within the memory arrays, the occupied area of all functional and addressable memory cells on the die having a total combined area which is no greater than 14 mm^2; and

peripheral circuitry and pitch circuitry formed on the die relative to the memory arrays; the peripheral circuitry electrically interconnecting with the pins and including operably interconnected control and timing circuitry, address and redundancy circuitry, data and test path circuitry, and voltage supply circuitry which collectively enable full access to all addressable memory cells of the memory arrays.

7. The semiconductor memory device of claim 6 wherein the peripheral circuitry, the pitch circuitry, and the memory arrays are fabricated to include a total of four or less composite conductive line layers.

8. The semiconductor memory device of claim 6 wherein the peripheral circuitry, the pitch circuitry and the memory arrays have a total combined continuous surface area on the die which is less than or equal to 35 mm^2.

9. The semiconductor memory device of claim 6 wherein the peripheral circuitry, the pitch circuitry, and the memory arrays are fabricated to include at least five composite conductive line layers, the occupied area of all functional and operable memory cells on the die having a total combined area on the die which is no greater than 11 mm^2.

10. The semiconductor memory device of claim 6 wherein the peripheral circuitry, the pitch circuitry, and the memory arrays are fabricated to include at least five composite conductive line layers; the peripheral circuitry, the pitch circuitry and the memory arrays having a total combined continuous surface area on the die which is less than or equal to 32 mm^2.

11. A semiconductor memory device comprising:

a semiconductor die encapsulated in a package, the package having an encapsulating body and electrically conductive interconnect pins extending outwardly from the body;

a total of no more than 4,500,000 functional and operably addressable memory cells arranged in multiple memory arrays formed on the die, the individual functional and operably addressable memory cells occupying area on the die within the memory arrays, the occupied area of all functional and addressable memory cells on the die having a total combined area which is no greater than 3.3 mm^2; and

peripheral circuitry and pitch circuitry formed on the die relative to the memory arrays; the peripheral circuitry electrically interconnecting with the pins and including operably interconnected control and timing circuitry, address and redundancy circuitry, data and test path circuitry, and voltage supply circuitry which collectively enable full access to all addressable memory cells of the memory arrays.

12. The semiconductor memory device of claim 11 wherein the peripheral circuitry, the pitch circuitry, and the memory arrays are fabricated to include a total of four or less composite conductive line layers.

13. The semiconductor memory device of claim 11 wherein the peripheral circuitry, the pitch circuitry and the memory arrays have a total combined continuous surface area on the die which is less than or equal to 11.0 mm^2.

14. The semiconductor memory device of claim 11 wherein the peripheral circuitry, the pitch circuitry, and the memory arrays are fabricated to include at least five composite conductive line layers, the occupied area of all functional and operable memory cells on the die having a total combined area on the die which is no greater than 2.5 mm^2.

15. The semiconductor memory device of claim 11 wherein the peripheral circuitry, the pitch circuitry, and the memory arrays are fabricated to include at least five composite conductive line layers; the peripheral circuitry, the pitch circuitry and the memory arrays having a total combined continuous surface area on the die which is less than or equal to 10.2 mm^2.

16. A semiconductor memory device comprising:

a semiconductor die encapsulated in a package, the package having an encapsulating body and electrically conductive interconnect pins extending outwardly from the body;

a total of no more than 68,000,000 functional and operably addressable memory cells arranged in multiple memory arrays formed on the die, at least one of the memory arrays containing at least 100 square microns of continuous die surface area having at least 128 of the functional and operably addressable memory cells; and

peripheral circuitry and pitch circuitry formed on the die relative to the memory arrays; the peripheral circuitry electrically interconnecting with the pins and including operably interconnected control and timing circuitry, address and redundancy circuitry, data and test path circuitry, and voltage supply circuitry which collectively enable full access to all addressable memory cells of the memory arrays.

17. The semiconductor memory device of claim 16 wherein at least one of the memory arrays containing at least 100 square microns of continuous die surface area having at least 170 of the functional and operably addressable memory cells.

18. A semiconductor memory device comprising:

a semiconductor die encapsulated in a package, the package having an encapsulating body and electrically conductive interconnect pins extending outwardly from the body;

a total of no more than 17,000,000 functional and operably addressable memory cells arranged in multiple memory arrays formed on the die, at least one of the memory arrays containing at least 100 square microns of continuous die surface area having at least 128 of the functional and operably addressable memory cells; and

peripheral circuitry and pitch circuitry formed on the die relative to the memory arrays; the peripheral circuitry electrically interconnecting with the pins and including operably interconnected control and timing circuitry, address and redundancy circuitry, data and test path circuitry, and voltage supply circuitry which collectively enable full access to all addressable memory cells of the memory arrays.

19. The semiconductor memory device of claim 18 wherein at least one of the memory arrays containing at least 100 square microns of continuous die surface area having at least 170 of the functional and operably addressable memory cells.

20. A semiconductor memory device comprising:

a semiconductor die encapsulated in a package, the package having an encapsulating body and electrically conductive interconnect pins extending outwardly from the body;

a total of no more than 4,500,000 functional and operably addressable memory cells arranged in multiple memory arrays formed on the die, at least one of the memory arrays containing at least 100 square microns of continuous die surface area having at least 128 of the functional and operably addressable memory cells; and

peripheral circuitry and pitch circuitry formed on the die relative to the memory arrays; the peripheral circuitry electrically interconnecting with the pins and including operably interconnected control and timing circuitry, address and redundancy circuitry, data and test path circuitry, and voltage supply circuitry which collectively enable full access to all addressable memory cells of the memory arrays.

21. The semiconductor memory device of claim 20 wherein at least one of the memory arrays containing at least 100 square microns of continuous die surface area having at least 170 of the functional and operably addressable memory cells.

22. A semiconductor memory device comprising:

a total of no more than 68,000,000 functional and operably addressable memory cells arranged in multiple memory arrays formed on a semiconductor die; and

circuitry formed on the semiconductor die permitting data to be written to and read from one or more of the memory cells, at least one of the memory arrays containing at least 100 square microns of continuous die surface area having at least 128 of the functional and operably addressable memory cells.

23. The semiconductor memory device of claim 22 wherein the total number of functional and operably addressable memory cells on the semiconductor die is no more than 17,000,000.

24. The semiconductor memory device of claim 22 wherein the total number of functional and operably addressable memory cells on the semiconductor die is no more than 4,500,000.

25. The semiconductor memory device of claim 22 wherein at least one of the memory arrays containing at least 100 square microns of continuous die surface area having at least 170 of the functional and operably addressable memory cells.

26. The semiconductor memory device of claim 22 wherein at least one of the memory arrays containing at least 100 square microns of continuous die surface area having at least 170 of the functional and operably addressable memory cells, and the total number of functional and operably addressable memory cells on the semiconductor die is no more than 17,000,000.

27. The semiconductor memory device of claim 22 wherein at least one of the memory arrays containing at least 100 square microns of continuous die surface area having at least 170 of the functional and operably addressable memory cells, and the total number of functional and operably addressable memory cells on the semiconductor die is no more than 4,500,000.